AMENDMENTS

I. IN THE SPECIFICATION:

Please replace paragraphs 0058 to 0061 with the following:

[0058] The system environment 700 may include several processors, of which only two, processors 740, 760 are shown for clarity. Processors 740, 760 may include level one (L1) caches 742, 762. The system environment 700 may have several functions connected via bus interfaces 744, 764, 712, 708 with a system bus 706. In one embodiment, system bus 706 may be the front side bus (FSB) utilized with Pentium.RTM. class microprocessors. In other embodiments, other busses may be used. In some embodiments memory ~~controller~~ center 734 and bus bridge 732 may collectively be referred to as a chip set. In some embodiments, functions of a chipset may be divided among physical chips differently from the manner shown in the system environment 700.

[0059] Memory ~~controller~~ center 734 may permit processors 740, 760 to read and write from system memory 710 and/or from a basic input/output system (BIOS) erasable programmable read-only memory (EPROM) 736. In some embodiments BIOS EPROM 736 may utilize flash memory. Memory ~~controller~~ center 734 may include a bus interface 708 to permit memory read and write data to be carried to and from bus agents on system bus 706. Memory ~~controller~~ center 734 may also connect with a high-performance graphics circuit 738 across a high-performance graphics interface [[739]]. In certain embodiments the high-performance graphics interface ~~739~~ may be an advanced graphics port (AGP) interface. Memory ~~controller~~ center 734 may direct read data from system memory 710 to the high-performance graphics circuit 738 across high-performance graphics interface ~~739~~.

[0060] The system environment 800 may also include several processors, of which only two, processors 770, 780 are shown for clarity. Processors 770, 780 (which include processor cores 774, 784) may each include a local memory channel hub (MCH) 772, 782 to connect with memory 702, 704. Processors 770, 780 may exchange data via a point-to-point interface [[750]] using point-to-point interface circuits ~~778, 788~~ 777, 787. Processors 770, 780 may each

exchange data with a chipset 790 via individual point-to-point interfaces ~~752, 754~~ using point to point interface circuits 776, 794, 786, [[798]] 797. Chipset 790 may also exchange data with a high-performance graphics circuit [[738]] 737 via a high-performance graphics interface 792.

[0061] In the system environment 700, bus bridge 732 may permit data exchanges between system bus 706 and bus 716, which may in some embodiments be a industry standard architecture (ISA) bus or a peripheral component interconnect (PCI) bus. In the system environment 800, chipset 790 may exchange data with a bus 716 via a bus interface 796. In either system, there may be various input/output I/O devices 714 on the bus 716, including in some embodiments low performance graphics controllers, video controllers, and networking controllers. Another bus bridge 718, 717 may in some embodiments be used to permit data exchanges between bus 716 and bus 720. Bus 720 may in some embodiments be a small computer system interface (SCSI) bus, integrated drive electronics (IDE) bus, or universal serial bus (USB) bus. Additional I/O devices may be connected with bus 720. These may include input devices 722, which may include, but are not limited to, keyboards, pointing devices, and mice, audio I/O 724, communications devices 726, including modems and network interfaces, and data storage devices 728, 727. Software code 730 may be stored on data storage device 728, 727. In some embodiments, data storage device 728, 727 may be, for example, but is not limited to, a fixed magnetic disk, a floppy disk drive, an optical disk drive, a magneto-optical disk drive, a magnetic tape, or non-volatile memory including flash memory.

Please insert the following after paragraph 0002 and before the "Brief Description of the Drawings" heading:

Brief Summary of the Invention

Checkpoints may be used to recover from branch mispredictions using scalable rename map table recovery.